DOUBLE RECESSED TRANSISTOR

Abstract of the Disclosure

A transistor structure is provided. This structure has a source electrode and a drain electrode. A doped cap layer of $Ga_xIn_{1-x}As$ is disposed below the source electrode and the drain electrode and provides a cap layer opening. An undoped resistive layer of $Ga_xIn_{1-x}As$ is disposed below the cap layer and defines a resistive layer opening in registration with the cap layer opening and having a first width. A Schottky layer of $Al_yIn_{1-y}As$ is disposed below the resistive layer. An undoped channel layer is disposed below the Schottky layer. A semi-insulating substrate is disposed below the channel layer. A top surface of the Schottky layer beneath the resistive layer opening provides a recess having a second width smaller than the first width. A gate electrode is in contact with a bottom surface of the recess provided by the Schottky layer.

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